DISCLOSURE TEXT:

2p. In certain data processing operations, it is desirable to transfer large blocks of data from one portion of the memory to another portion and also to gather or scatter data to or from noncontiguous locations in memory. When certain modifications are provided, the central processor can perform these functions. However, such data transfers can be time consuming and it is desirable not to unduly burden the central processor in this manner.
- Channels or peripheral control units are provided in data processing systems to relieve the central processor of the control of data transfer to or from peripheral devices according to a control word format. A special storage channel can be provided to relieve the central processor of control of data transfer in bulk form from one memory location to another. Such an operation is initiated by the central processor upon execution of a single instruction. In response to this execution, the selected storage channel retrieves a command control word from main storage through an indirect addressing method.
- This control word is gated to the A register of the storage channel from which the respective fields thereof are gated to appropriate monitoring registers. These fields include a data address which, at this time, is employed to specify the location in memory for a second control word, a flag field to indicate, among other things, command chaining, and a control command.
 The second
control word is retrieved and provides the fields for a position address which is the location in main storage of the first element of one of the fields in storage to or from which data is to be transferred, a length which is the number of elements located sequentially in that field to constitute a subset, and a displacement which is the number of consecutive addresses between the highest addressable element of one subset and the lowest addressable element

of the adjacent higher addressable subset.
-        Because of the command chaining flag, a third control word is
retrieved from main storage and placed in the A register and
specifies a data address. This represents the first addressable
address of the second conceptual field and a count which represents
the total number data address. This represents the first addressable
address of the second conceptual field and a count which represents
the total number of words in that respective data field. Thus,
sufficient information is transferred to the channel to allow it to
control transfer from one of the conceptual fields to the other
conceptual field. Such transfer is dependent upon the operation
specified by the control command of the last selected control word.
-        The central processor having been released to continue its own
program, the storage channel proceeds to utilize the A and B
registers to fetch data from one of the above described conceptual
fields in storage ad then to request access to the other conceptual
field according to the corresponding addresses for the respective
fields that are updated as the data transfer occurs. The sequence
for fetching ad storing data can be as follows:
F(a), F(b), S(a), F(a), S(b), F(b), S(a), ...F(b), S(a), S(b). F(a)
is a data fetch for register A, F(b) is a data fetch for register B,
S(a) is a data store from register A, and S(b) is a data store from
register B.
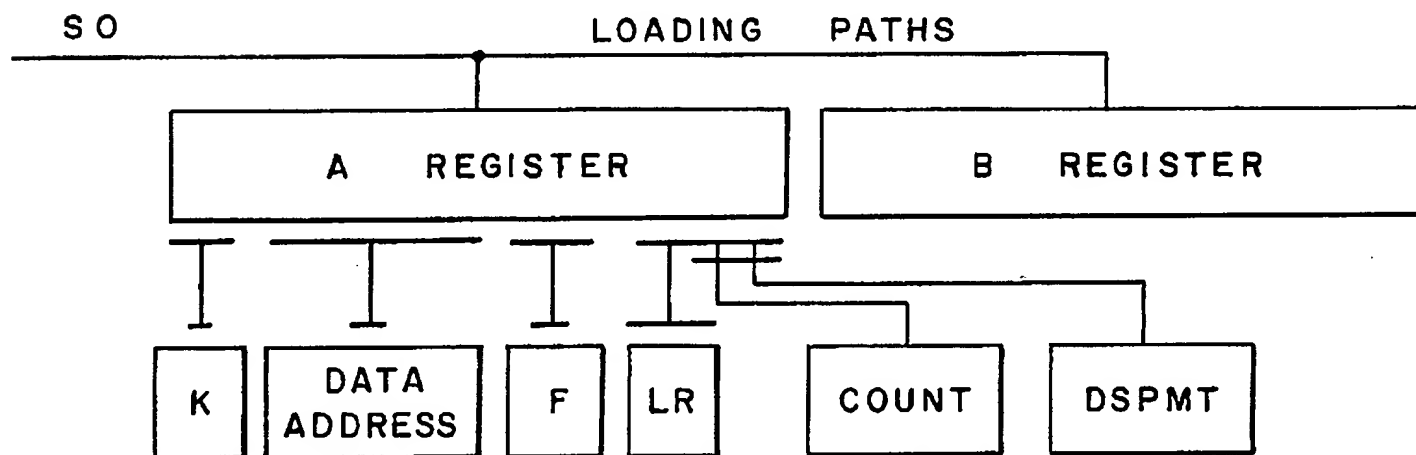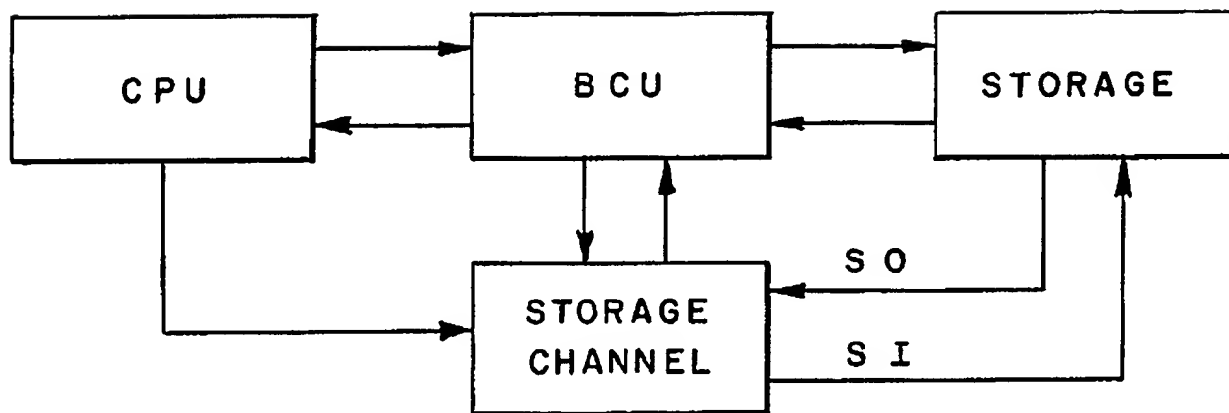
K   =   PROTECTION KEY REGISTER
F   =   FLAG REGISTER
LR =   LENGTH REGISTER
DSPMT = DISPLACEMENT REGISTER
S O   =   STORAGE DATA BUSS OUT
S I   =   STORAGE DATA BUSS IN